I²C High-efficiency Bidirectional Buck-Boost Controller

1. Description

The SW3203 is a high-efficiency synchronous 4-transistor bidirectional buck-boost controller that supports 3V-28V input voltage and 3V-22V output voltage, I2C and FB control methods, and 2-channel load access detection and 3-channel NMOS drive. It can be used in a variety of application scenarios and can simplify the solution design.

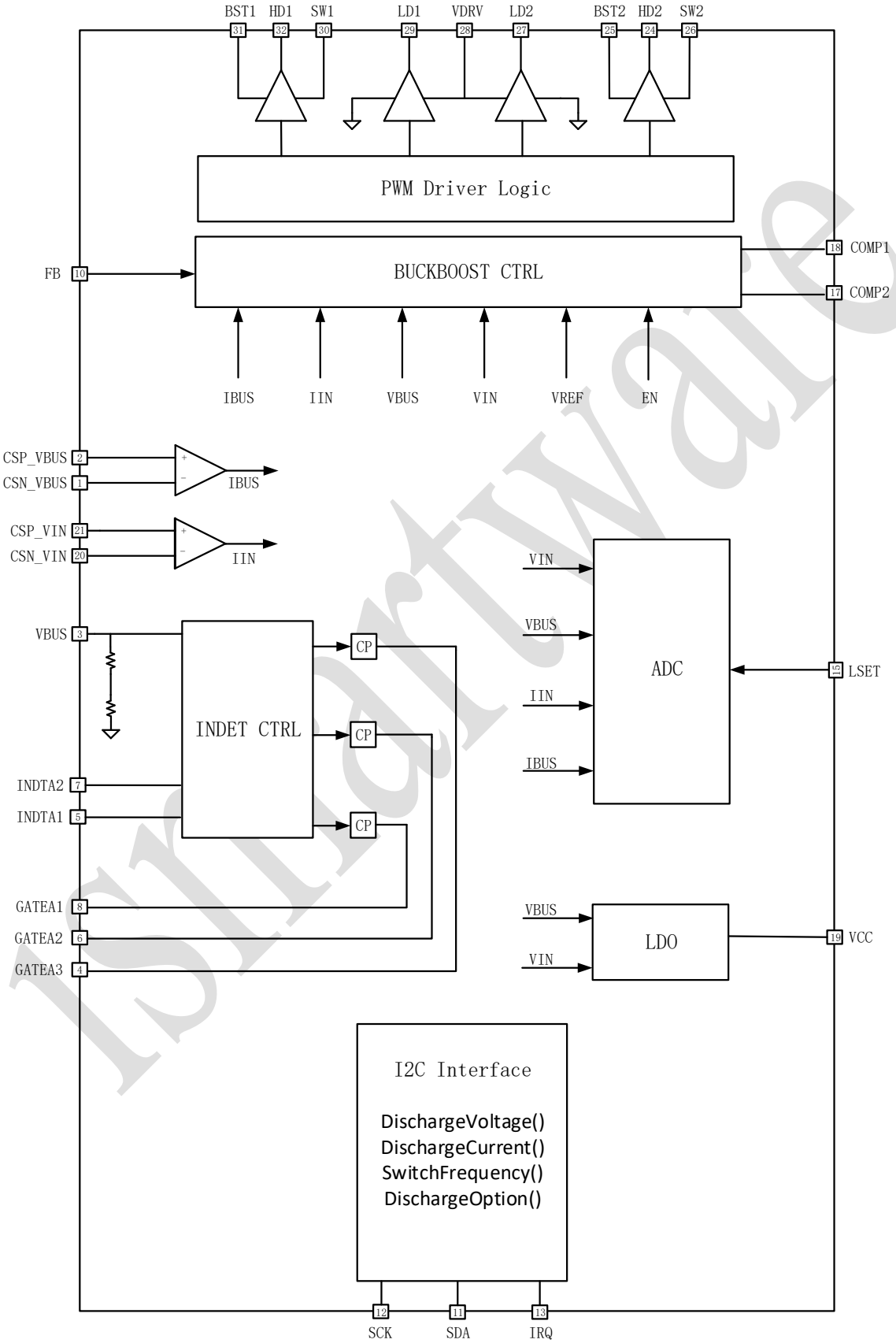
2. Applications

- Car Charger
- Electronic Cigarette
- Adapter
- USB Hub
- Smart USB Power Strip
- Industrial Equipment

3. Features

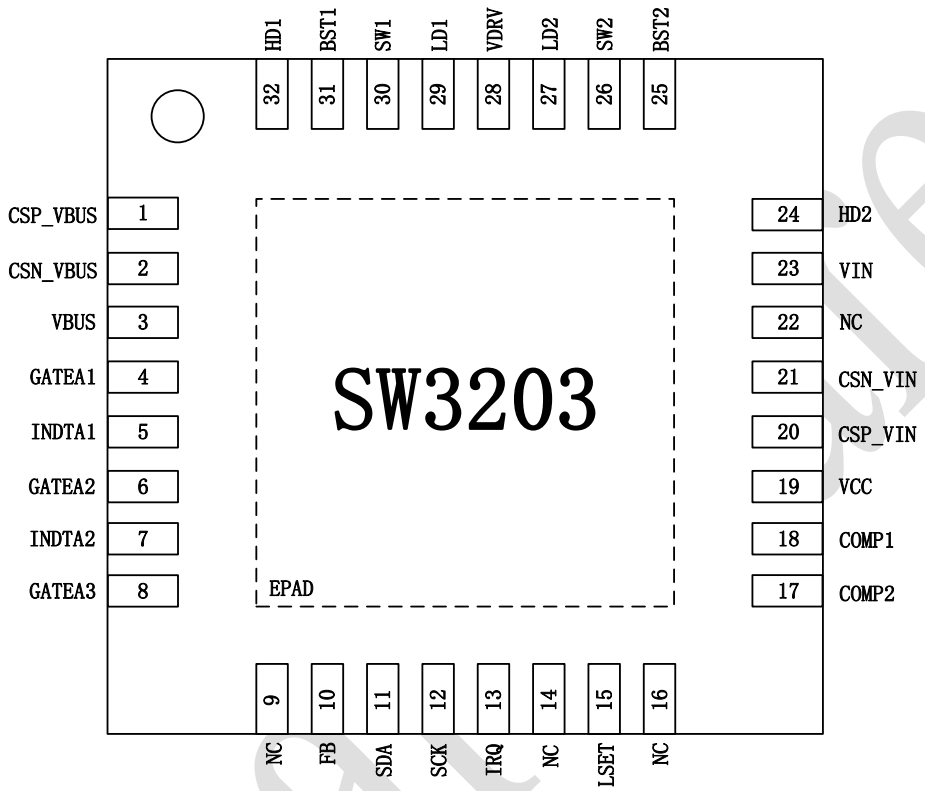
- **Reverse Buck-boost Discharge**
  - Support 100W output power
  - Support 3V-24V input voltage
  - Support 3V-22V output voltage
  - Flexible selection of FB/I2C voltage regulation mode
  - Support 200KHz/300KHz/400KHz/ 800KHz switching frequency
  - Support I2C programming to control Output current limit
  - Automatic PFM/PWM mode
  - Seamless switching between boost and buck
- **Port Connect Detection**
  - 2 load inserting detection points
- **12bit High Precision ADC**
- **Low Quiescent Input Current**
  - Shutdown current down to 40uA
- **Path MOS Driver**
  - 3 NMOS drivers integrated
- **Protection**
  - Input Over Voltage Protection
  - Output Over Voltage Protection
  - Output Over Current Protection
  - Output Short Protection
  - Thermal shutdown protection
- **I2C Interface**
- **QFN-32(4x4mm) Package**

4. Functional Block Diagram



5. Pin Configuration and Functions

5.1. Pin Configuration



5.2. Pin Functions

Pin	Name	Function Description
1	CSP_VBUS	The current sensing negative pole on the VBUS side. In order to avoid the influence of high-frequency noise on the current sensing signal and to stabilize the current sensing, a 100nF capacitor needs to be added in parallel with the VBUS current sensing resistor, and a low-pass filter needs to be added between the current sensing resistor and CSP_VBUS. For the design of the low-pass filter, please refer to "10.2.4 VBUS current sensing low-pass filter parameter selection".
2	CSN_VBUS	The current sensing positive pole on the VBUS side. In order to avoid the influence of high-frequency noise on the current sensing signal and to stabilize the current sensing, a 100nF capacitor needs to be added in parallel with the VBUS current sensing resistor, and a low-pass filter needs to be added between the current sensing resistor and CSN_VBUS. For the

		design of the low-pass filter, please refer to "10.2.4 VBUS current sensing low-pass filter parameter selection".
3	VBUS	Chip power supply and VBUS voltage sensing.
4	GATEA1	NMOS power path transistor driver 1. This driver is enabled by a charge pump, which is weak in driving capability. When the path transistor drive is used, it is recommended to use an NMOS with gate source leakage current no greater than 100nA. The GATEA1 can remain floating without using the power path transistor drive.
5	INDTA1	Load inserting detection 1. When this function is used to detect load inserting, a ground capacitor of no less than 4.7uF must be set on INDTA1, and the recommended value of this capacitor is 10uF.
6	GATEA2	NMOS power path transistor driver 2. This driver is enabled by a charge pump, which is weak in driving capability. When the path transistor driver is used, an NMOS with gate source leakage current no greater than 100nA is recommended. The GATEA2 can remain floating without using the pass transistor drive.
7	INDTA2	Load inserting detection 2. When this function is used to detect load inserting, a grounded capacitor of no less than 4.7uF must be set on INDTA2, and the recommended value of this capacitor is 10uF.
8	GATEA3	NMOS power path transistor driver 3. This driver is enabled by a charge pump, which is weak in driving capability. When the power path transistor driver is used, an NMOS with gate source leakage current no greater than 100nA is recommended. The GATEA3 can remain floating without using the power path transistor drive.
9	NC	Floating.
10	FB	External feedback of VBUS output voltage. The voltage of the FB is fixed at 0.5V. When the output voltage is not set with external feedback, the FB is floating.
11	SDA	I2C Data. Please connect SDA to the host controller. 10KΩ pull-up resistors are recommended for SDA lines.
12	SCK	I2C Clock. Please connect SCK to the host controller. 10KΩ pull-up resistors are recommended for SCK lines.
13	IRQ	I2C Interrupt. IRQ is for open-drain output. 10KΩ resistors are recommended. When the event interrupt is triggered, the IRQ output goes low until the event interrupt flag bit is cleared.
14	NC	Floating.

15	LSET	Inductance value setting: 4 different inductance values can be set: 1uH for 10KΩ, 2.2uH for 20KΩ, 3.3uH for 30KΩ, and 4.7uH for 43KΩ. This setting must be consistent with the external inductance value; otherwise the buck-boost cannot work normally.
16	NC	Floating.
17	COMP2	CC loop compensation. For the specific RC compensation network of COMP2, please refer to "10.2.3 COMP RC parameter selection".
18	COMP1	CV loop compensation. For the specific RC compensation network of COMP1, please refer to "10.2.3 COMP RC parameter selection"
19	VCC	5V linear regulator output provided by VBUS or VIN. The 5V linear regulator is activated when the buck-boost is operating. VCC needs a 10uF ground capacitor near the VCC pin of the chip.
20	CSP_VIN	The current sensing positive pole on the VIN side; VIN voltage sensing. In order to ensure the stability of current sensing, a 100nF capacitor needs to be added in parallel with the VIN current sensing resistor.
21	CSN_VIN	The current sensing negative pole on the VIN side. In order to ensure the stability of current sensing, a 100nF capacitor needs to be added in parallel with the VIN current sensing resistor.
22	NC	Floating.
23	VIN	Chip power supply; VIN voltage sensing.
24	HD2	VIN side upper transistor gate drive. It needs to be connected to the gate of the high-side NMOS (Q4) of the half-bridge on the VIN side.
25	BST2	VIN side upper transistor bootstrap. A 100nF capacitor needs to be connected between SW2 and BST2. The bootstrap diodes of VDRV and BST2 are integrated inside the chip.
26	SW2	VIN side switching point. SW2 needs to be connected to the source of the high-side NMOS (Q4) of the half-bridge on the VIN side.
27	LD2	VIN side lower transistor gate drive. It needs to be connected to the gate of the low-side NMOS (Q3) of the half-bridge on the VIN side.
28	VDRV	5.5V linear regulator output provided by VBUS or VIN. The 5.5V linear regulator is activated in standby mode and buck-boost operating mode. VDRV needs a 10uF ground capacitor near the VDRV pin of the chip.

29	LD1	VBUS side lower transistor gate drive. It needs to be connected to the gate of the low-side NMOS (Q2) of the half-bridge on the VBUS side
30	SW1	VBUS side switching point. SW1 needs to be connected to the source of the high-side NMOS (Q1) of the half-bridge on the VBUS side.
31	BST1	VBUS side upper transistor bootstrap. A 100nF capacitor needs to be connected between SW1 and BST1. The bootstrap diodes of VDRV and BST1 are integrated inside the chip.
32	HD1	VBUS side upper transistor gate. It needs to be connected to the gate of the high-side NMOS (Q1) of the half-bridge on the VBUS side.
/	EPAD	The grounded pad of the chip needs to be connected to the power ground plane to maintain proper connection between the EPAD and the PCB, thus ensuring its working performance and good heat dissipation.

6. Absolute Maximum Ratings

Parameters	Symbol	MIN	MAX	UNIT
VBUS Port Voltage	VBUS/FB/CSN_VBUS/ CSP_VBUS	-0.3	35	V
VIN Port Voltage	CSN_VIN/CSP_VIN/ VIN	-0.3	35	V
Switch Driver Voltage	HD1/HD2/BST1/BST2	-0.3	40	V
Switch Port Voltage	SW1/SW2	-0.3	35	V
Port Voltage	INDTA1/INDTA2	-0.3	35	V
Path Control Voltage	GATEA1/GATEA2/ GATEA3	-0.3	40	V
Another pin voltages		-0.3	7	V
Junction temperature		-40	+150	°C
Storage temperature		-60	+150	°C
ESD（HBM）		-4	+4	KV

【Notice】Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maxi mum rated conditions for extended periods my affect device reliability.

7. Recommended Operating Conditions

Parameters	Symbol	MIN	Typical	MAX	UNIT
Input Voltage Range	VIN	4		28	V
Output Voltage Range	VBUS	3		22	V

8. Electrical Characteristics

（VIN = 24V, VBUS = 12V, T_A = 25°C, unless otherwise specified.）

Parameters	Symbol	Test Conditions	MIN	TYP	MAX	UNIT
Power Supply						
VIN input voltage	V_{INDTB}		3		28	V
VIN input undervoltage threshold	V_{IN_UVLO}	INDTB voltage falling		3		V
VIN input undervoltage hysteresis	$V_{IN\_UVLO\_HYS}$	INDTB voltage rising		400		mV
VDRV output voltage	V_{DRV}	Buck-Boost operating、Standby	5.3	5.5	5.7	V

		Shutdown		0		V
VDRV current limit	I_{VDRV}	Buck-Boost operating、Standby	35	50		mA
		Shutdown		0		mA
VCC output voltage	V_{CC}	Buck-Boost operating	4.8	5	5.2	V
		Standby、Shutdown		3.9		V
VCC current limit	I_{VCC}	Buck-Boost operating	90	120		mA
		Standby、Shutdown		10		mA
Discharge Mode						
VBUS output voltage range	V_{DISCHG_VOL}	I2C voltage regulation mode dischg_vbus=0x000~0x7ff	3		22	V
VBUS output voltage	V_{DISCHG_VOL}	I2C voltage regulation mode dischg_vbus=0x0C8	-3%	5	+3%	V
		I2C voltage regulation mode dischg_vbus=0x2BC	-2%	10	+2%	V
		I2C voltage regulation mode dischg_vbus=0x6A4	-2%	20	+2%	V
FB voltage	V_{FB}	FB voltage regulation mode	-2%	0.5	+2%	V
VBUS discharge current limit range	$I_{CC\_DISCHG\_VBUS}$	dischg_ibus_limit=0x00~0xff	0.5		6.85	A
VBUS discharge current limit	$I_{CC\_DISCHG\_VBUS}$	dischg_ibus_limit=0x00	0.4	0.5	0.7	A
		dischg_ibus_limit=0x0A	0.9	1	1.25	A
		dischg_ibus_limit=0x32	2.85	3	3.35	A
		dischg_ibus_limit=0x5A	4.8	5	5.4	A
		dischg_ibus_limit=0x78	6.3	6.5	7	A
VIN discharge current limit range	$I_{CC\_DISCHG\_VIN}$	dischg_iin_limit=0x00~0x77	0.1		12	A
VIN discharge current limit	$I_{CC\_DISCHG\_VIN}$	dischg_iin_limit=0x04	0.3	0.5	0.7	A
		dischg_iin_limit=0x13	1.8	2	2.2	A
		dischg_iin_limit=0x31	4.7	5	5.3	A
		dischg_iin_limit=0x4A	7.1	7.5	7.9	A
		dischg_iin_limit=0x63	9.5	10	10.5	A
Quiescent Current						
Shutdown current	$I_{Q\_SHUTDOWN}$	Disable Load Inserting detection、Disable standby		40	80	uA

		mode				
		Enable Load Inserting detection、Disable standby mode		50	100	uA
Standby current	$I_{Q\_STANDBY}$	Disable Load Inserting detection、Eaable standby mode		530	900	uA
		Enable Load Inserting detection、Eaable standby mode		540	920	uA
VIN input current without load	I_{DISCHG_NOLOAD}	VIN=12V、VBUS=5V、800KHz、Qg=5.5nC		1.9		mA
		VIN=12V、VBUS=12V、800KHz、Qg=5.5nC		2.3		mA
		VIN=12V、VBUS=20V、800KHz、Qg=5.5nC		3.4		mA
Switching						
Switching frequency	F_{SW}	Buck-Boost operating、freq=0x1	150	200	250	kHz
		Buck-Boost operating、freq=0x0	230	300	370	kHz
		Buck-Boost operating、freq=0x2	300	400	500	kHz
		Buck-Boost operating、freq=0x3	650	800	900	kHz
Abnormality protection						
VBUS overvoltage protection	$V_{VBUS\_DISCHG\_OVP}$	VBUS rising、I2C voltage regulation mode	V_{DISCHG_VOL}*109.5%	V_{DISCHG_VOL}*112.5%	V_{DISCHG_VOL}*115.5%	V
		VBUS falling、I2C voltage regulation mode		V_{DISCHG_VOL}*106%		V
		VBUS rising、FB voltage regulation mode	23.2	24	24.8	V
		VBUS falling、FB voltage regulation mode		22.7		V
VBUS overload protection	$V_{VBUS\_DISCHG\_OLP}$	VBUS falling、I2C voltage regulation mode		V_{DISCHG_VOL}*80%		V
		VBUS falling、FB voltage regulation mode		1.76		V
VBUS short-circuit protection	$V_{VBUS\_DISCHG\_SCP}$	VBUS falling		1.76		V

VIN overvoltage protection	$V_{VIN\_DISCHG\_OVP}$	VIN rising	25.2	26	26.8	V
		VIN falling		24.6		V
Thermal shutdown threshold	T_{DIE_OTP}	Chip temperature rising		150		℃
Thermal shutdown hysteresis	$T_{DIE\_OTP\_HYS}$	Chip temperature falling		20		℃
Automatic Detection（LSET）						
Detection threshold of 4.7UH inductance	$V_{LSET\_4.7UH}$		1.75		2.5	V
Detection threshold of 3.3UH inductance	$V_{LSET\_3.3UH}$		1.25		1.75	V
Detection threshold of 2.2UH inductance	$V_{LSET\_2.2UH}$		0.75		1.25	V
Detection threshold of 1UH inductance	V_{LSET_1UH}		0.25		0.75	V
I2C						
I2C Clock frequency	F_{I2C_CLK}			100	400	kHz
I2C pulse width low	V_{IL}				0.75	V
I2C pulse width high	V_{IH}		1.2			V

9. Function Description

The SW3203 is a high-efficiency synchronous 4-transistor bidirectional buck-boost controller that supports 3V-28V input voltage and 3V-22V output voltage, I2C and FB control methods, and 2-channel load access detection and 3-channel NMOS drive. It can be used in a variety of application scenarios and can simplify the solution design.

The SW3203 supports the shutdown low-power mode, in which the minimum leakage current is down to 40uA. It can be used for applications with high static power consumption. The SW3203 can also protect the device against output short circuit, output overcurrent, output overvoltage, over temperature and other abnormalities.

9.1. Buck-Boost

Under different VBUS and VIN voltages, the SW3203 will automatically work in three modes: buck, buck-boost, and boost. The three modes can be switched seamlessly, and there will be no sudden change in VBUS voltage in the switching process. In addition, the SW3203 supports PFM/PWM. Under light load, it works in the PFM mode; under heavy load, it works in the PWM mode. At the same time, SW3203 supports 4 inductance values (1uH, 2.2uH, 3.3uH and 4.7uH) and 4 switching frequencies (200K, 300K, 400K and 800K), which can be flexibly adjusted according to the performance needs in actual applications.

9.1.1. Pulse frequency modulation (PFM)

In order to improve the efficiency at light load, the SW3203 will work in the PFM mode. The actual switching frequency will decrease when the charging power and discharging power decrease. When the average inductor current reaches the PWM mode set value, the SW3203 will switch from PFM to PWM.

In addition, although working in the PFM mode improves the light-load efficiency, the output ripple will increase accordingly. For applications that are sensitive to output ripple, the forced PWM mode can be set through the register. In the forced PWM mode, the SW3203 will not enter PFM even when operating at light load.

9.1.2. Pulse width modulation (PWM)

When operating in the PWM mode, at the beginning of a cycle, when the output of the error amplifier is higher than the ramp voltage, the high-side NMOS of the half-bridge will be turned on; and when the output of the error amplifier falls below the ramp voltage, the low-side NMOS of the half-bridge will be turned on. At the end of the cycle, the ramp voltage is reset and ready to start the next cycle. In the process of switching on the MOS, the principle of “turning off before turning on” must be always followed to avoid the dangerous situation that high-side and low-side NMOS transistors are both on. With both the high-side and low-side NMOS transistors off, the inductor current is maintained by the body diodes of the high-side or low-side NMOS transistors.

The following table shows the operating states of the four power MOS transistors Q1-Q4 in the PWM mode.

PWM Mode			
Mode	Buck	Buck-Boost	Boost
Q1	On	Switching	Switching
Q2	Off	Switching	Switching
Q3	Switching	Switching	Off
Q4	Switching	Switching	On

9.2. Discharge settings

The SW3203 supports the external FB voltage regulation and internal I2C voltage regulation, and it is compatible with different protocol chips.

9.2.1. Start discharging

The SW3203 is set to the FB mode by default. The output is automatically turned on when powered on. The IBUS output current limit is set to 5.3A, while the IIN current limit is set to 12A.

In addition, the default state of the SW3203 can also set to I2C mode, in which, the SW3203 will not automatically turn on the output when it is powered on. To turn on the output, please follow the steps below:

(1) Set the output voltage.

(2) Set the VBUS/VIN output current limit value.

(3) Enable the discharge.

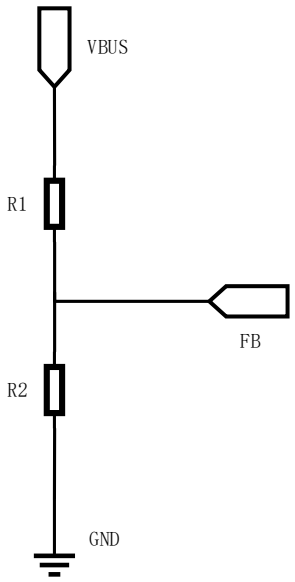
The I2C and FB modes can be modified through registers, but whether to automatically turn on the output after power-on depends only on the default state at power-on.

9.2.2. FB voltage regulation

In the external FB voltage regulation mode, the voltage of the FB pin is fixed at 0.5V, and an appropriate voltage divider can be selected according to the required output voltage. 100K is recommended for R1.

In the FB mode, the output voltage is calculated as follows：

$$\mathrm{VBUS} = 0.5 \times (1 + \frac{R1}{R2})$$



For the settings of output current limit, please refer to "9.2.3 I2C voltage regulation" for details.

9.2.3. I2C voltage regulation

In the internal I2C voltage regulation mode, the FB pin is in the floating state, and there is no need to add an FB resistor. After setting the output voltage and output current limit threshold, the output can be turned on by enabling the discharge enable bit.

The VBUS output voltage can be set through the register discchg_vbus[10:0] in the range of 3V-22V (10mV/step).

The VBUS current limit can be set through the register discchg_ibus_limit[6:0] in the range of 0.5A-6.85A (50mA/step).

The VIN current limit can be set through the register discchg_iin_limit[6:0] in the range of 0.1A-12A (100mA/step). When dischg_iin_limit[6:0]=0x00, the VIN current limit is set to 0.1A.

9.3. Abnormality protection

The SW3203 is designed with effective protection measures, including thermal shutdown protection, cycle-by-cycle peak overcurrent protection, VIN undervoltage protection, VIN overvoltage protection, VBUS overvoltage protection, VBUS short-circuit protection, VBUS overcurrent protection, etc., to ensure the safety of charging and discharging equipment to the greatest extent.

9.3.1. Thermal shutdown protection

The SW3203 supports thermal shutdown protection. When its temperature rises to the thermal shutdown protection threshold and lasts for more than 16ms, it is considered that the chip over-temperature abnormality is triggered and the buck-boost will be turned off. There are 4 levels of chip over-temperature temperature for selection: 120°C/130°C/140°C/150°C. After the chip over-temperature protection is triggered, as long as the chip temperature drops to the thermal shutdown threshold -20°C and lasts for more than 16mS, the chip will exit the thermal shutdown and the buck-boost will restart.

9.3.2. VBUS overvoltage protection

The SW3203 supports VBUS overvoltage protection. When the output voltage exceeds the VBUS overvoltage protection threshold and lasts for more than 16ms, it is considered that the VBUS overvoltage abnormality is triggered, and the discharge will be turned off. After triggering the VBUS overvoltage abnormality, when the output voltage is lower than the VBUS overvoltage exit threshold for more than 16ms, the VBUS overvoltage abnormality will be exited and the discharge will be resumed.

In the FB voltage regulation mode, the VBUS overvoltage protection threshold is 24V, and the VBUS overvoltage exit threshold is 22.74V.

In the I2C voltage regulation mode, the VBUS overvoltage protection threshold is 112% of the set output voltage, and the VBUS overvoltage exit threshold is 106% of the set output voltage.

9.3.3. VBUS overload protection

The SW3203 supports VBUS overload protection in discharge mode, which can turn off the output when the output is overloaded. When the VBUS discharging voltage is lower than the VBUS overcurrent protection threshold and lasts for 32ms, it is considered that the VBUS overcurrent

abnormality is triggered and the discharge will be turned off. When the discharge turn off，the hiccup function will starts every other period of time，hiccup interval time can be set to 200mS or 500mS through the register.

In the FB voltage regulation mode, the VBUS overcurrent protection threshold is consistent with the short-circuit protection threshold, i.e., 1.76V.

In the I2C voltage regulation mode, the discharging VBUS overcurrent protection threshold is 80% of the set output voltage.

9.3.4. VBUS short-circuit protection

The SW3203 supports VBUS short-circuit protection, which can turn off the buck-boost output when a short circuit occurs at the output. When the VBUS output voltage is lower than the output VBUS short-circuit protection threshold and lasts for more than 4ms, it is considered that the discharging VBUS short-circuit abnormality is triggered, and the discharge will be turned off. When the discharge turn off，the hiccup function will starts every other period of time，hiccup interval time can be set to 200mS or 500mS through the register.

The output VBUS short-circuit protection threshold is 1.76V.

9.3.5. VIN undervoltage protection

The SW3203 supports discharging VIN undervoltage protection, which can turn off the buck-boost output e when the input voltage is low. When the input voltage is lower than the VIN undervoltage protection threshold and lasts for more than 32ms, it is considered that the discharging VIN undervoltage abnormality is triggered and the discharge will be turned off. When the input voltage is higher than the VIN undervoltage protection threshold plus the VIN undervoltage protection hysteresis and lasts for more than 64ms, the VIN undervoltage abnormality will be terminated and the discharge will be resumed.

The VIN undervoltage protection threshold is 3V. The VIN undervoltage protection hysteresis is 0.4V.

9.3.6. VIN overvoltage protection

The SW3203 supports VIN overvoltage protection, which can prohibit the discharge in the case of overvoltage at the VIN input. When the input voltage is higher than the VIN overvoltage protection threshold and lasts for more than 100us, it is considered that the VIN overvoltage abnormality is triggered and the discharge will be turned off. After triggering the VIN overvoltage protection, when the input voltage is lower than the VIN overvoltage recovery threshold and lasts for more than 36ms, it is considered that the VIN overvoltage abnormality is terminated.

The VIN overvoltage protection threshold is 26V, while the VIN overvoltage recovery threshold is 24.63V.

9.3.7. Cycle-by-cycle peak overcurrent protection

The SW3203 supports cycle-by-cycle peak overcurrent protection. During the operation of the buck-boost, if the peak inductor current exceeds 12A/14A/16A/18A, the active transistor in the current mode will be turned off in advance to limit the peak inductor current.

When working in the discharging boost mode, the SW3203 detects the peak current of the inductor with the Vds of Q2 and complete the cycle-by-cycle peak overcurrent protection. It is required to set the register of the on-resistance of Q2 according to the actual on-resistance of Q2 to ensure the actual

detected peak current limit of the inductor to be closer to the inductor peak current value set by the register. The register of the on-resistance of Q2 can be set to 2.5mΩ/5mΩ/7.5mΩ/10mΩ. The actual peak current limit value in the discharging boost mode is as follows.

$$I_{OCP\_ACT} = \frac{R_{DSON\_Q2\_SET}}{R_{DSON\_Q2\_ACT}} \times I_{OCP\_SET}$$

where in I_{OCP_ACT} is the actual peak current limit value, $R_{DSON\_Q2\_ACT}$ is the actual on-resistance of Q2, $R_{DSON\_Q2\_SET}$ is the on-resistance of Q2 set by the register, and I_{OCP_SET} is the peak current limit value set by the register.

9.4. ADC

The SW3203 has a built-in 12bit ADC, which can collect data such as VBUS/VIN/IBUS/IIN. The specific calculation formula is as follows.

Channel	Description	Dynamic range	Calculation formula (N is the ADC output code value)
Vin	VIN voltage	0V-30.72V	Vin=N*7.5mV
Vbus	VBUS voltage	0V-30.72V	Vbus=N*7.5mV
Iin_dischg	VIN discharging current	0A-20.48A	Iin_dischg=N*5mA
Ibus_dischg	VBUS discharging current	0A-20.48A	Ibus_dischg=N*5mA
Tdie	On-chip temperature	-100℃~200℃	Tdiet=(N-1839)/6.82℃

9.5. IRQ

The SW3203 integrates the external interrupt pin IRQ in an open-drain structure. When it is used, a 10K resistor is recommended to pull up. When an event that needs to be monitored occurs, the IRQ will pull low and remain low until the flag bit of the corresponding event is cleared.

The events that can be monitored include adapter input pull-out, load detection trigger and operation abnormality. Each event can be individually set through registers.

9.6. Inserting detection

The SW3203 integrates two-channel load inserting detection, so that it can automatically identify external load inserting when it is turned on, which simplifies the solution design.

When inserting detection is turned on, the voltage on the corresponding port will be established above the detection threshold, and the load inserting will pull down this voltage to below the identification threshold, thereby identifying the device inserting.

After each inserting detection is triggered, if you want to continue to identify the external load inserting, you need to turn off the inserting detection and then turn it on again to take effect.

9.7. Power path transistor driver

The SW3203 integrates 3 NMOS power path transistor drivers, each of which can be turned on and off independently without adding any external circuit, which simplifies the design.

9.8. I2C

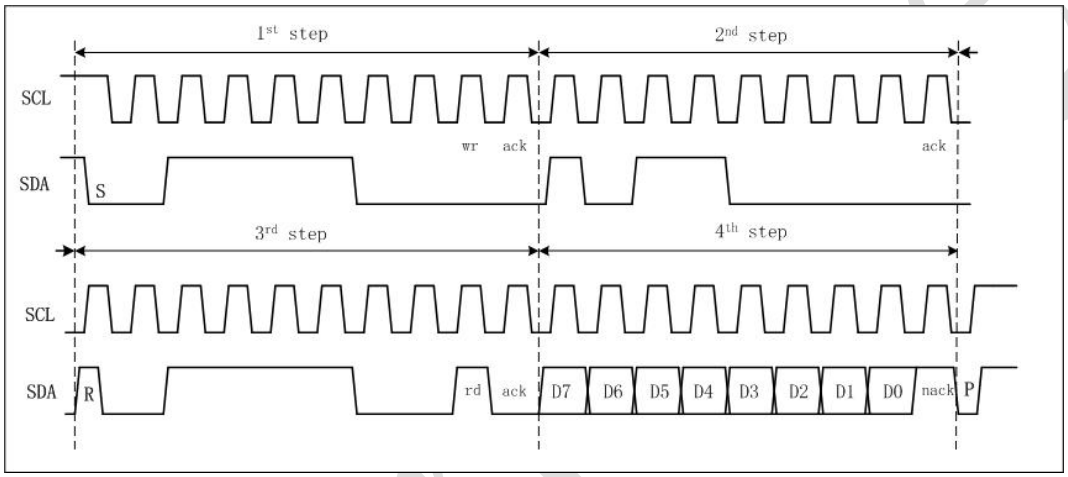
The SW3203 supports I2C interface and 100K-400K transmission rate. The master can read the status information of the chip through the I2C interface. And the SW3203 supports 4 different I2C addresses: 0x3C/0x38/0x1C/0x18.

I2C does not support continuous read/write.

Read:

Slave address: 0x3C (read 0x79, write 0x78)

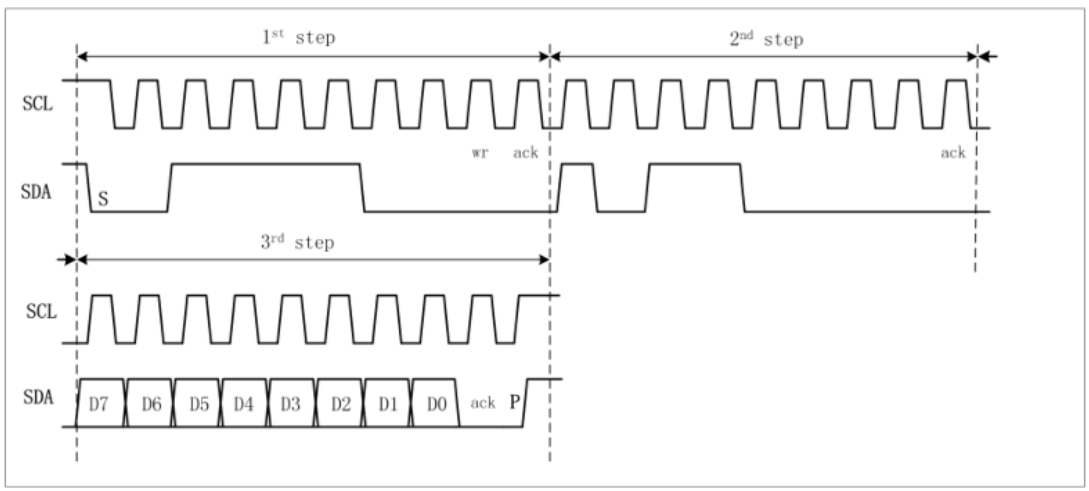
Register address: 0xB0



Write:

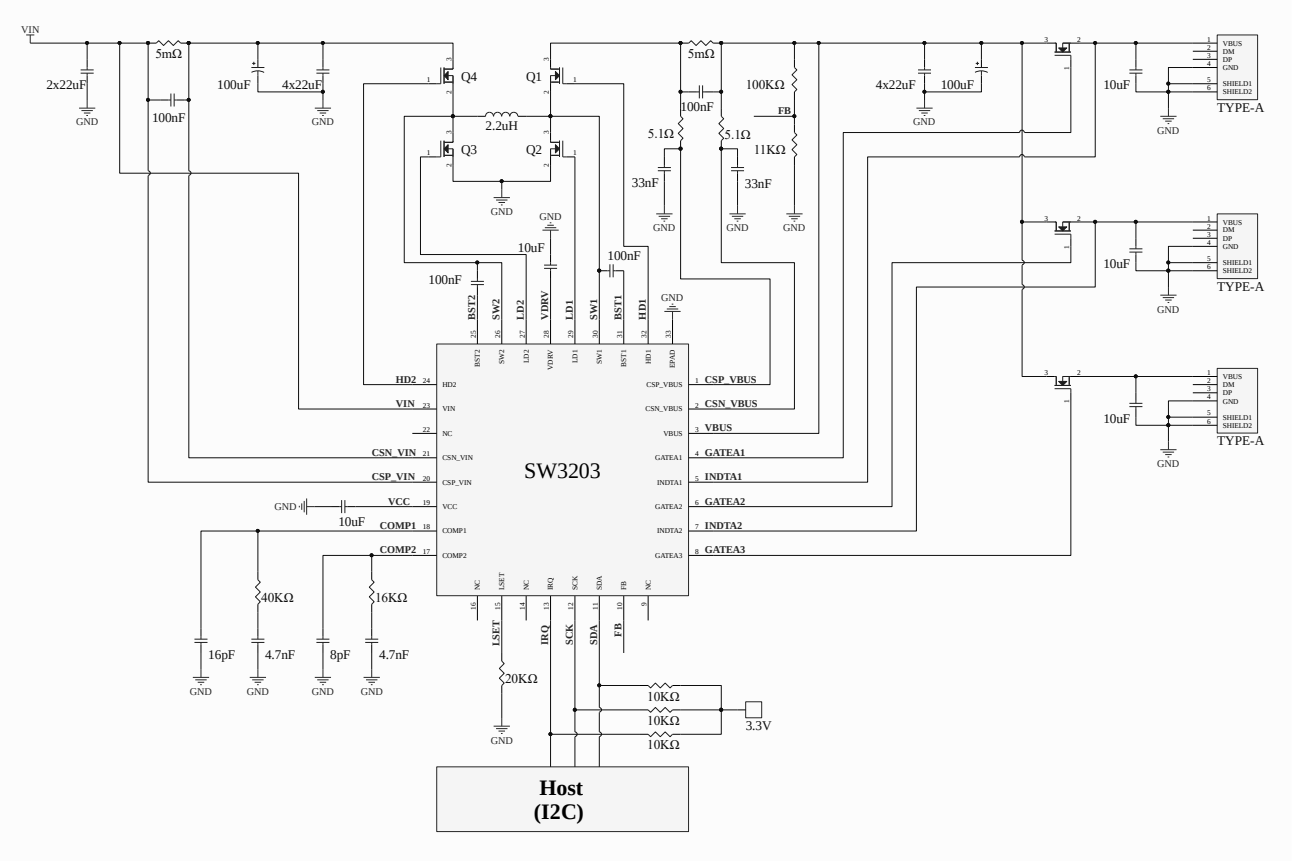
Slave address: 0x3C (read 0x79, write 0x78)

Register address: 0xB0



10. Application and Implementation

10.1. Typical Application



10.2. Parameter configuration

10.2.1. Inductor value selection

LSET is connected to ground with different resistors for configuring the inductors. When the switching frequency is 800K, 1uH or 2.2uH inductors can be selected and 100uF solid state capacitors are recommended for VIN and VBUS. When the switching frequency is 200K/300K/400K, 3.3uH or 4.7uH inductors are recommended and the solid state capacitors for VIN and VBUS should be increased to 220uF.

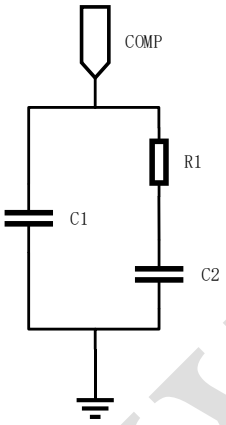
Please refer to the table below for specific resistor settings of the LSET.

LSET resistor	Inductor value
10K	1uH
20K	2.2 uH
30K	3.3 uH
43K	4.7 uH

10.2.2. COMP RC parameter selection

Different resistance and capacitance parameters should be selected for the COMP1 and COMP2 pins according to different inductances. COMP1 is the CV loop compensation pin, while COMP2 is the CC loop compensation pin.

COMP compensation circuit:



Specific settings of COMP1:

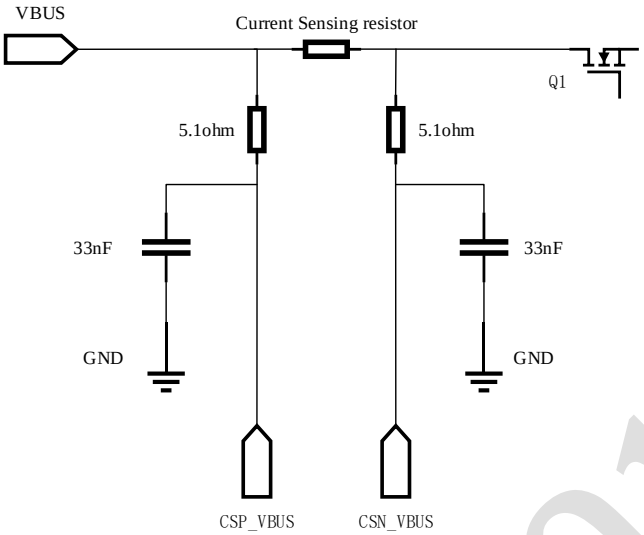
Inductor value	R1	C1	C2
1uH	60K	16pF	4.7nF
2.2 uH	40K	16pF	4.7nF
3.3 uH	30K	16pF	4.7nF
4.7 uH	20K	16pF	4.7nF

Specific settings of COMP2:

Inductor value	R1	C1	C2
1uH	8K	8pF	4.7nF
2.2 uH	16K	8pF	4.7nF
3.3 uH	24K	8pF	4.7nF
4.7 uH	32K	8pF	4.7nF

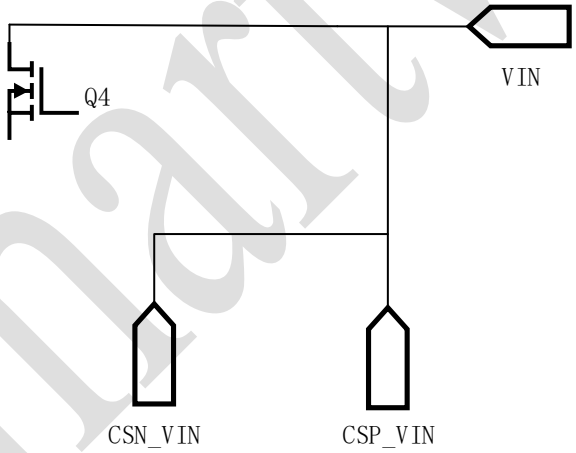
10.2.3. VBUS current sensing low-pass filter parameter selection

The SW3203 is designed based on the average current mode and it monitors the inductor current through the VBUS current sensing resistors. The parasitic inductance on the PCB leads to high-frequency noise on CSN_VBUS-CSP_VBUS, which affects the current sensing. When the time constant of the low-pass filter is between 47ns and 200ns, it can filter out high-frequency noise sufficiently, and will not cause too much delay to the current sensing signal, thus ensuring stable operation. The filter circuit shown in the figure below is recommended to be added on CSN_VBUS and CSP_VBUS.



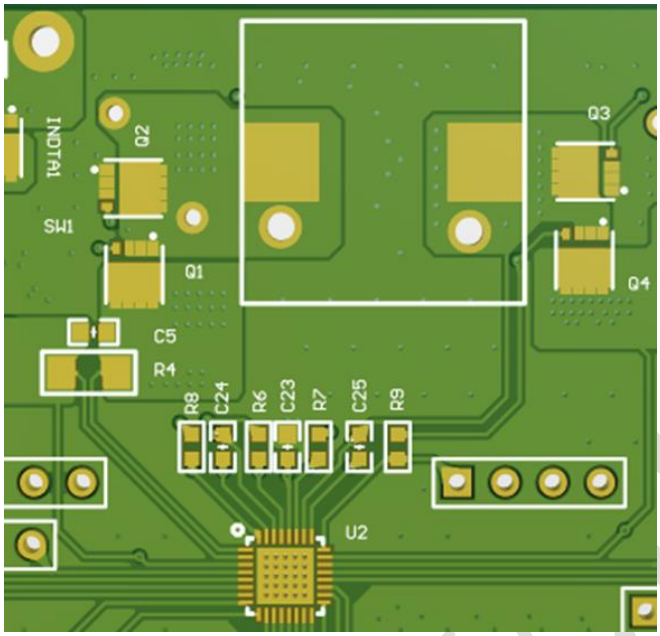
10.2.4. VIN current sensing

In the application, if the VIN current limit protection is not used, the current sensing resistor on the VIN side can be removed, and CSP_VIN and CSN_VIN can be shorted to VIN. The specific circuit connection is shown in the figure below.

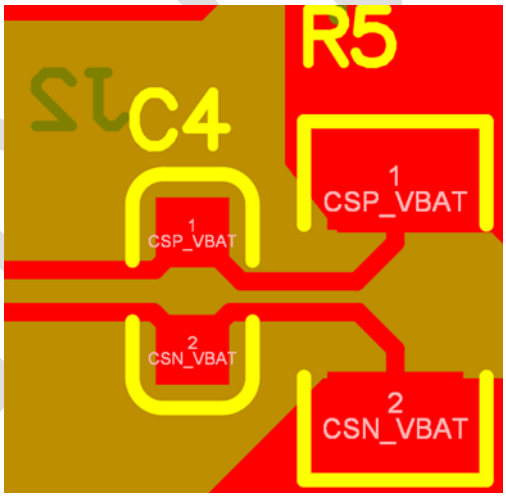


11. PCB Layout Reference

1. Power MOS transistors and inductors, as the main heat generating devices, should be kept away from each other and heat dissipation measures should be taken; Q1~Q4 power MOS transistors are recommended to be placed on the same side of the chip.



2. Kelvin connection should be used to arranging the current sensing traces, pulling them inward from the resistor pad and leading to the CSP_VIN and CSN_VIN pins separately, without leading to other places in the route. Similarly, traces on the VBUS side, with a width of 8 mil or 10 mil, should be directly connected to the CSP_VBUS and CSN_VBUS pins through the sensing resistors; the 0.1uF capacitor in parallel with the sensing resistor is placed near the sensing resistor.



3. General signal traces (not carrying high currents) should have a width of 0.2mm (8mil) or 0.25mm (10mil), and other traces from the chip's HD1, LD1, SW1, HD2, LD2, and SW2 pins to the power components should be at least 0.25mm (10mil) or more in width.
4. Since the high frequency of signal flip at the inductor may affect other signal lines, traces should not be arranged below the bottom of the inductors if possible.
5. The VCC/VDRV capacitors and COMP1/COMP2 compensation networks should be placed near the IC pins.
6. The input capacitors should be as close as possible to the power supply of the power MOS transistors

and ground connection, with the shortest possible path;

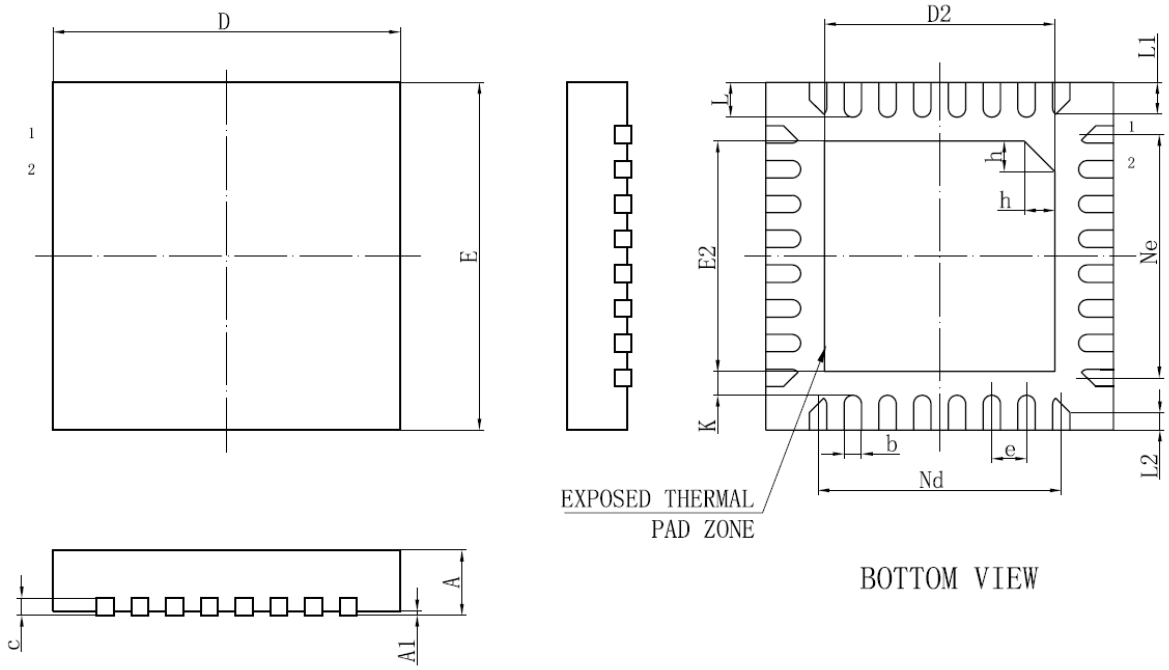
7. The feedback resistors need to be placed near the FB pins and away from noise sources.

8. The traces of VBUS, SW1, SW2, B+, and GND should be as wide as possible, copper pours are recommended, and the width should not be less than 80mil; the traces of SW should be as short as possible, without change layers. At least 12 vias are needed when high-current network traces change layers. Make as many vias as possible, while considering the integrity of the underlying ground and heat dissipation.

9. The number of vias should be determined based on the size of the overcurrent and the size of the heat dissipation pad when changing layers. More than 12 vias are recommended for VBUS, SW1, SW2, B+ and GND to change layers; more vias are recommended in other spare spaces to strengthen the connection between the bottom layer and the top layer and to facilitate heat dissipation.

12. Mechanical and Packaging

12.1. Package Summary



12.2. Package Outline and Dimensions

Symbol	Dimension in Millimeters		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	3.90	4.00	4.10
D2	2.55	2.65	2.75
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.55	2.65	2.75
L	0.3	0.40	0.5
L1	0.25	0.35	0.45
L2	0.15	0.20	0.25
h	0.30	0.35	0.40

13. Revision History

V1.0 Initial version.
V1.1 Package Outline and Dimensions is modified.

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